Amendments to the Claims:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Previously presented) Mirror suppression circuit comprising

a first quadrature signal path coupled between quadrature signal input and output terminals and including

an error correction circuit for correction of amplitude and phase errors in a carrier modulated quadrature signal comprising a pair of in-phase and phase quadrature signal components,

wherein

a quadrature output of the error correction circuit is coupled through a first filter circuit for a selection of the quadrature signal to a first quadrature input of an error detection circuit,

the first quadrature signal path is coupled prior to the first filter circuit through a second quadrature signal path to a second quadrature input of the error detection circuit,

the error detection circuit detects amplitude and phase errors and provides amplitude and phase control signals to amplitude and phase control inputs of the error correction circuit for a negative feed back of the amplitude and phase errors to the error correction circuit,

the amplitude control signal varies with at least one of products I_w*I_{ref} and Q_w*Q_{ref}, and

the phase control signal varies with at least one of products I_w*Q_{ref} and Q_w*I_{ref},

I_w and Q_w representing the in-phase and phase quadrature signal components of the quadrature signal at the first quadrature input of the error detection circuit, and

I_{ref} and Q_{ref} representing the in-phase and phase quadrature signal components of a quadrature reference signal occurring at the negative carrier frequency of the quadrature signal at the second quadrature input of the error detection circuit.

2. (Previously presented) Mirror suppression circuit according to claim 1, wherein
the amplitude control signal varies with $I_w*I_{ref} + Q_w*Q_{ref}$, and
the phase control signal varies with $I_w*Q_{ref} - Q_w*I_{ref}$.

3. (Previously presented) Mirror suppression circuit according to claim 1, wherein
the second quadrature signal path includes
an inverter that provides signal inversion in obtaining the quadrature reference signal.

4. (Previously presented) Mirror suppression circuit according to claim 1, wherein
the second quadrature signal path is coupled to the first quadrature signal path subsequent to the error correction circuit.

5. (Previously presented) Mirror suppression circuit according to claim 1, wherein
the second quadrature signal path includes a second filter circuit for a selection of the quadrature reference signal.

6. (Previously presented) Mirror suppression circuit according to claim 3, wherein
the second quadrature signal path includes the inverter coupled between the first quadrature signal path and the second filter circuit,
the second filter circuit being substantially identical to the first filter circuit.

7. (Previously presented) Receiver providing quadrature signal processing comprising

an RF input stage subsequently followed by a mixer stage for a conversion of an RF signal into an IF signal,

an IF stage for a selective amplification of the IF signal, and

a mirror suppression circuit comprising

a first quadrature signal path coupled between quadrature signal input and output terminals and including

an error correction circuit for correction of amplitude and phase errors in a carrier modulated quadrature signal comprising a pair of in-phase and phase quadrature signal components,

wherein

a quadrature output of the error correction circuit is coupled through a first filter circuit for a selection of the quadrature signal to a first quadrature input of an error detection circuit,

the first quadrature signal path is coupled prior to the first filter circuit through a second quadrature signal path to a second quadrature input of the error detection circuit,

the error detection circuit detects amplitude and phase errors and provides amplitude and phase control signals to amplitude and phase control inputs of the error correction circuit for a negative feed back of the amplitude and phase errors to the error correction circuit,

the amplitude control signal varies with at least one of products I_w*I_{ref} and Q_w*Q_{ref},

the phase control signal varies with at least one of products I_w*Q_{ref} and Q_w*I_{ref},

I_w and Q_w representing the in-phase and phase quadrature signal components of the quadrature signal at the first quadrature input of the error detection circuit, and

I_{ref} and Q_{ref} representing the in-phase and phase quadrature signal components of a quadrature reference signal occurring at the negative carrier

frequency of the quadrature signal at the second quadrature input of the error detection circuit,

the quadrature signal input of the mirror suppression circuit is coupled to a quadrature output of the mixer stage, and

the first filter circuit is part of the IF stage and has a resonance frequency at the carrier frequency of the IF signal.

8. (Previously presented) Receiver according to claim 7, wherein

the second quadrature signal path includes a second filter circuit for a selection of the quadrature reference signal, and

the second filter circuit selects the quadrature reference signal occurring at the negative carrier frequency of the quadrature IF signal.

9. (Previously presented) Receiver according to claim 8 wherein

the second quadrature signal path includes

an inverter that provides signal inversion in obtaining the quadrature reference signal, and

the second quadrature signal path comprises

the inverter coupled between the first quadrature signal path and the second filter circuit,

the second filter circuit being identical to the IF filter circuit.

10. (Previously presented) Receiver according to claim 9, wherein

both first and second filter circuits comprise resonance amplifier type polyphase filters.

11. (Previously presented) Receiver according to claim 7, wherein

the error correction circuit includes

an amplitude correction circuit comprising

a first multiplier included in at least one of the pair of in-phase and quadrature paths of the first quadrature signal path for an amplitude variation of the signal at the input with the amplitude error.

12. (Previously presented) Receiver according to claim 11, wherein

the amplitude correction circuit comprises

a differential stage following the detection circuit that converts the amplitude control signal into a differential pair of first and second amplitude control signals and supplies the differential pair to the first and a second multiplier, respectively,

the first and second multipliers are included in the in-phase and quadrature paths of the first quadrature signal path.

13. (Previously presented) Receiver according to claim 7, wherein

the error correction circuit includes a phase correction circuit comprising

a third multiplier having

a signal input coupled to one of the in-phase and quadrature paths of the first quadrature signal path and

a signal output coupled to a first adder device, which is included in the other of the in-phase and quadrature paths for supplying thereto a part of the signal occurring at the one path to the other path varying with the phase control signal.

14. (Previously presented) Receiver according to claim 13, wherein

the phase correction circuit comprises

a differential stage following the detection circuit that converts the phase error into a differential pair of first and second phase error signals and supplies the differential pair to modulation signal inputs of the third and a fourth multiplier, respectively, and

the third and fourth multipliers include:

inputs coupled to the phase quadrature and in-phase paths of the first quadrature signal path, and

outputs coupled to the first and a second adder device, which are included in the in-phase and phase quadrature paths, respectively.

15. (Previously presented) Mirror suppression circuit according to claim 2, wherein

the second quadrature signal path includes

an inverter that provides signal inversion in obtaining the quadrature reference signal.

16. (Previously presented) Mirror suppression circuit according to claim 15, wherein

the second quadrature signal path is coupled to the first quadrature signal path subsequent to the error correction circuit.

17. (Previously presented) Mirror suppression circuit according to claim 16, wherein

the second quadrature signal path includes a second filter circuit for a selection of the quadrature reference signal.

18. (Previously presented) Mirror suppression circuit according to claim 17, wherein the second quadrature signal path includes the inverter coupled between the first quadrature signal path and the second filter circuit,

the second filter circuit being substantially identical to the first filter circuit.

19. (Previously presented) Mirror suppression circuit according to claim 2, wherein the second quadrature signal path is coupled to the first quadrature signal path subsequent to the error correction circuit.

20. (Previously presented) Mirror suppression circuit according to claim 3, wherein the second quadrature signal path is coupled to the first quadrature signal path subsequent to the error correction circuit.